UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,440	12/04/2003	Ken G. Pomaranski	200209695-1	6842

22879 7590 07/29/2005

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
BUI, BRYAN	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 07/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/727,440	POMARANSKI ET AL.	
	Examiner	Art Unit	
	Bryan Bui	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☒ Claim(s) *20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *62005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicants' papers filed on 6/24/2005 have been received and entered. Claims 1-20 are pending in the application.

2. Applicants' remark has been considered but it is moot in the new ground of the rejection.

3. It is noted that the term "de-allocated" and re-allocated" as recited in claim 13 is considered as inherently known in the computer technology (Microsoft press Computer Dictionary, third edition) by not reserve a resource/to free previously allocated memory (de-allocated); and the allocation of memory to a process or program or reserve a resource (re-allocated).

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-6, 8-9, 11, 17-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Coyle et al. (6609221).

With respect to claims 1-6, and, 17, Coyle et al teach a computer system having an interconnect test module comprising a processor configured to cause an operating system to be booted and interconnect (figure 1, column 5, lines 13-29), a first test unit

(first test device) coupled to the interconnect, and a second test unit (second test device) coupled to the interconnect (figure 1, column 5, lines 13-29); wherein the first test unit is configured to provide a test pattern to the second test unit on the interconnect in response to a signal from the operating system (column 5, lines 33-41, column 6, lines 1-8); a second test unit is configured to detect an error in the interconnect in response to receiving the test pattern and notifying (indicating, reporting) the operating system in response to detecting an error (column 6, lines 5-33).

With respect to claims 8-9, 11 Coyle et al teach the first component comprises a processor, and wherein the second component comprises a controller coupled to the processor and controller include a system controller, and controller comprises a memory controller (column 5, lines 12-38, column 11,lines 31-50); wherein the first component comprises an input/output (I/O) controller, and the second component comprises an input/output (I/O) device coupled to the I/O controller through an expansion slot (column 12, lines 7-27, further see Microsoft Press, Computer Dictionary, Third Edition "expansion slot" as inherent known to system bus for communicate as a socket in the computer system).

With respect to claims 18-19, Coyle et al teach a first switch couple to first test unit wherein a first component coupled to a first switch; a second switch coupled to a second test unit, wherein a second component coupled to a second switching component, the first test unit configured to cause the first switching mechanism to disconnect the first component from the interconnect, and the second test unit is

configured to cause the second switching mechanism to disconnect the second component from the interconnect (figures 1, 4A and column 9, lines 20-65).

3. Claims 13-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Lin et al. (6757803).

With respect to claims 13-14, Lin et al teach a computer system having an interconnect test module (figures 1) comprising causing a component (processor/memory/storage, etc) coupled to an interconnect to be de-allocated from use by an operating system and performing a test on the interconnect causing the component to be re-allocated to use by the operating system subsequent to performing the test (column 1, lines 7-13, column 9, lines 2-29); notifying the operating system in response to detecting an error in performance the test (column 7, lines 7-20).

With respect to claims15-16, Lin et al teach reporting results of the test to the operating system (column 4, lines 1-17); performing the test on the interconnect by providing test patterns on the interconnect (column 4, lines 39-53, column 10, line 45 to column 11, line 33).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 10, 12, 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coyle et al (US 6609221) in view of Lin et al (US 6757803).

With respect to claims 13-14, Coyle et al teaches a computer system having an interconnect test module comprising a processor configured to cause an operating system to be booted and interconnect (figure 1, column 5, lines 13-29), performing a test on the interconnect through the test units (first and second test devices) coupled to the interconnect (figure 1, column 5, lines 13-29); and notifying (indicating, reporting) the operating system in response to detecting an error (column 6, lines 5-33). Coyle et al does not mention a step of causing a component coupled to an interconnect to be de-allocated from use by an operating system and causing the component to be re-allocated to use by the operating system subsequent to performing the test. Line et al, however teach these limitations (column 9, lines 23-29, and column 10, lines 15-23). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Coyle et al' teachings to include a process to cause the component coupled to an interconnect to be de-allocated by an operating system as taught by Lin et al in order to recovery of memory in a computer system to avoiding loss of regions of memory by failure of the process to return allocated memory after finishing with it so that the region of memory can be de-allocated for re-use (column 1, lines 6-13).

With respect to claims 15-16, Coyle et al teach reporting results of the test to the operating system (column 9, lines 9-19); performing the test on the interconnect by providing test patterns on the interconnect (column 9, lines 24-43).

With respect to claims 10 and 12, Coyle et al teach the features of the claimed invention as set forth above, Coyle et al does not mention the operating to cause the processor to be de-allocated and provide the second signal to the first test module in

response to causing the processor to be de-allocated and the operating system to cause the expansion slot to be de-allocated and configured to provide the second signal to the first test module in response to causing the expansion slot to be de-allocated. Lin et al teach these limitations (column 9, lines 23-29, and column 10, lines 15-23). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Coyle et al' teachings to include a process to cause the component coupled to an interconnect to be de-allocated by an operating system, and the operating system causing the expansion slot (socket in interface bus of the computer system) as taught by Lin et al in order to recovery of memory in a computer system to avoiding loss of regions of memory by failure of the process to return allocated memory after finishing with it so that the region of memory can be de-allocated for re-use (column 1, lines 6-13).

Allowable Subject Matter

6. Claim 20 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bryan Bui whose telephone number is 571-272-2271. The examiner can normally be reached on M-Th from 7am-4pm, and Alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John E. Barlow can be reached on 571-272-2269. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BRYAN BUI
PRIMARY EXAMINER

BB

7/21/2005